SESSION 23 – TAPA III
Digital Building Blocks

Saturday, June 19, 8:00 a.m.
Chairpersons: S. Butler, AMD
H. Kabuo, Matsushita

23.1 — 8:00 a.m.

A Dynamic CAM-based on a One-Hot-Spot Block Code-for Millions-Entry Lookup, S. Hanzawa, T. Sakata, K. Kajigaya*, R. Takemura and T. Kawahara, Hitachi, Ltd., Tokyo, Japan, *Elpida Memory, Inc., Kanagawa, Japan

We have developed a one-hot-spot block code and three circuit techniques to realize large-scale and low-power CAMs. The proposed code efficiently stores IP addresses and reduces the entry count down by 52% on average. A hierarchical match-line structure and an on-chip entry compression/ extraction scheme enable the proposed code to be applied to our new CAM. Furthermore, a search-depth control scheme reduces power consumption down by 45%. The proposed dynamic CAM effectively achieves 1.5 million entries.

23.2 — 8:25 a.m.

A 90nm 6.5GHz 128x64b 4-Read 4-Write Ported Parameter Variation Tolerant Register File, A. Agarwal, K. Roy, S. Hsu*, R.K. Krishnamurthy* and S. Borkar*, Purdue University, West Lafayette, IN, *Intel Corporation, Hillsboro, OR

This paper describes a 128x64b 4-read, 4-write ported register file for 6.5GHz operation in 1.2V 90nm CMOS technology. A wordline underdrive technique combined with local bitline merge NAND whose P/N skew is optimally programmable based on die leakage enables 12% faster performance with 20% reduction in delay variation and 5x reduction in robustness failing dies over optimized high performance conventional implementation.

23.3 — 8:50 a.m.

An Automatic Direction Control Scheme for Bi-Directional Bus Repeaters with Dynamic Collaborative Driving, M. Nomura, T. Ohsawa, K. Takeda, Y. Nakazawa, Y. Hirota, Y. Hagihara and N. Nishi, NEC Corporation, Kanagawa, Japan

This paper describes a newly developed automatic direction-control-scheme for bi-directional bus repeaters with dynamic-collaborative-driving. Repeater directions are rapidly determined by detecting the direction of enable signal propagation through an additional enable signal line, which is driven by dynamic collaborative-drivers. Application to an on-chip peripheral bus reduced control circuits to half and a dynamically reconfigurable processor (DRP, a kind of innovative reconfigurable logic LSI) application could reduce configuration context data and transistor count to 25 %. Experimental results from a 0.18-um CMOS implementation indicate that the proposed scheme improves signal propagation time four times faster than a conventional 3-state busdriver scheme.

23.4 — 9:15 a.m.

A 16Gb/s Adaptive Bandwidth On-chip Bus Based on Hybrid Current/Voltage Mode Signaling, R. Bashirullah, W. Liu, R. Cavin* and D. Edwards*, North Carolina State University, Raleigh, NC, *Semiconductor Research Corporation, Research Triangle Park, NC

An adaptive bandwidth bus (ABB) uses both current and voltage sensing techniques to improve interconnection delay and signaling bandwidth compared to conventional static busses. Attaining a maximum aggregate bandwidth of 16Gb/s(i.e. 1Gb/s per line) across lossy on-chip interconnects spanning 1.75cm in length, the bus core fabricated in TSMC 0.35μm CMOS technology dissipates approximately 93mW with a supply of 2.5V and signal activity of 0.5. Experimental results indicate a reduction in power of 50% over current-mode (CM) sensing, and an improvement in interconnection delay and signaling bandwidth of 35%-70% and 66% over voltage-mode (VM) sensing, respectively.

23.5 — 9:40 a.m.

A Mixed Signal Rotator/Shifter for 8GHz Intel® Pentium® 4 Integer Core, A.P. Singh, M. Barany and D.J. Deleganes, Intel Corporation, Hillsboro, OR

A novel mixed signal 32-bit Rotator/Shifter circuit design enabling ultra-short latency Intel® Netburst™ Rotate and Shift instructions is described. Compared to previous generation Intel® Pentium® 4 processor designs, this implementation cuts Rotate/Shift latency and throughput by 75% while adding significant frequency headroom. The circuit manufactured on Intel's 90nm process confirms a significant boost in integer performance.

Break 10:05 a.m.